Miniaturized and Broadband V-band Balanced Frequency Doubler for Highly Integrated 3-D MMIC

Kenjiro Nishikawa, Belinda Piernas*, Tadao Nakagawa, and Katsuhiko Araki

NTT Network Innovation Laboratories, 1-1 Hikari-no-oka, Yokosuka, 2390847, Japan
*Now with Fujitsu Compound Semiconductor, Inc.

Abstract — **This paper presents a compact V-band balanced frequency doubler 3-D MMIC with broadband performance. The MMIC was fabricated by combining a commercial 0.15 μm GaAs pHEMT technology with the 3-D MMIC technology. A fabricated frequency doubler MMIC, which occupies 0.92 mm^2, achieves 2.5-dBm output power and more than 15-dB fundamental signal suppression over 50-GHz to 68-GHz (30% bandwidth) for an 8-dBm input signal. A transmit MMIC, intended for 50-GHz application, realizes a 10-dBm output power and 40-dB isolation in an area of 1.48 mm^2, it is supported by input and output buffer amplifiers. These fabricated MMICs are very effective in realizing compact and highly integrated single-chip transceiver MMICs. Furthermore, they can be re-used for various V-band applications, resulting in significant cost reduction.**

I. Introduction

Several millimeter-wave wireless communication systems have been proposed and developed for consumer applications in recent years. V-band applications with higher transmission bit rates, above 100 Mbps, require low-cost, highly integrated, and compact MMICs to realize simple packaging and low-cost RF products. A significant advantage is achieved when all RF components can be integrated on the same chip. A frequency multiplier is a key component to realize a single-chip millimeter-wave transceiver MMIC.

Reported V-band frequency doublers [1]-[6] that use single or balanced configuration are large and have restricted frequency bands, resulting in high-cost multi-chip configurations. Furthermore, the narrow bandwidth requires new designs or modification when developing new systems. This lengthens the development time excessively.

To realize a frequency doubler that offers both miniaturization and broadband operation, we use Marchand balun that consists of broadside couplers [7] and the three-dimensional (3-D) MMIC technology to achieve high integration level [8].

This paper presents compact V-band frequency doubler MMICs with broadband operation. The MMICs are fabricated by combining a commercial 0.15 μm GaAs pHEMT technology with the 3-D MMIC technology. The doubler MMICs are easily integrated to form single-chip transceiver MMICs because of their compactness. In addition, their broad bandwidths allow us to re-use them in various applications.

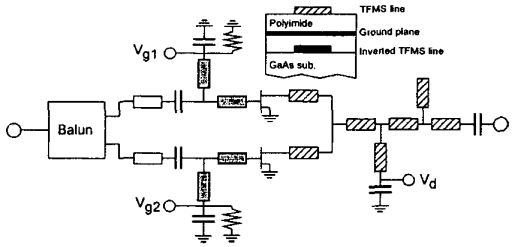


Fig. 1. Equivalent circuit of fabricated V-band balanced frequency doubler.

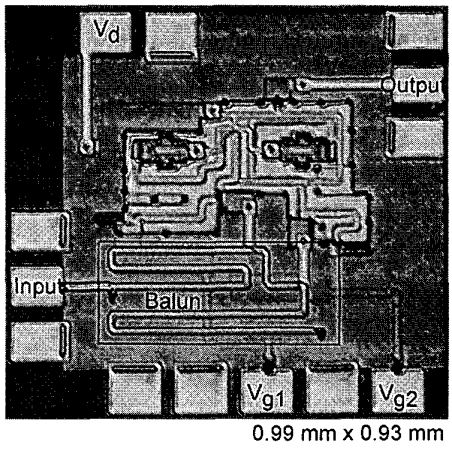


Fig. 2. Microphotograph of fabricated doubler MMIC.

II. Fabrication Technology

To develop these MMICs, we use a process technology combined with a commercial foundry process (UMS

0-7803-7239-5/02/$10.00 © 2002 IEEE

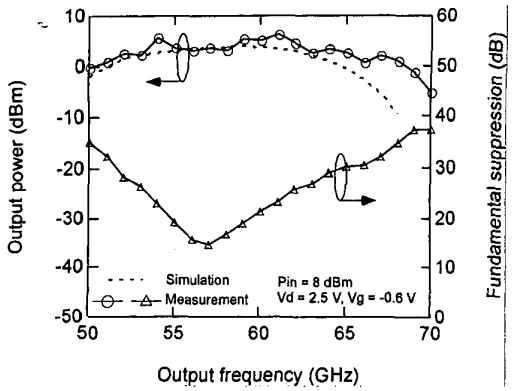


Fig. 3. Measured performance of doubler MMIC.

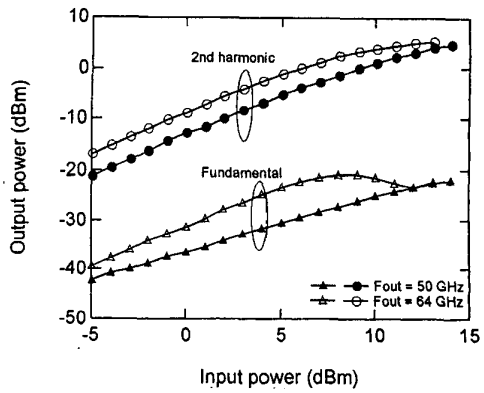


Fig. 4. Output power response at 50 GHz and 64 GHz.

PH15) from United Monolithic Semiconductor S.A.S. (UMS) with a 3-D MMIC interconnection process from NTT Electronics Corp. (NEL) that was originally developed by NTT Laboratories [9]. After finishing the UMS PH15 process, the 3-D MMIC interconnection process using four layers of 2.5-μm polyimide film was performed on PH15 GaAs wafers delivered from UMS. Transistor performances after the 3-D process remain high (f_T > 110 GHz, f_{max} > 170 GHz) despite the increase in parasitic capacitance around the transistor gate.

III. Doubler Design

To realize broadband and compact frequency doublers, we use compact compensated Marchand balun [7] as a 180-degree divider and the stacked configuration of input/output matching circuits. The compensated Marchand balun consists of two broadside couplers and a short transmission line to connect them. The transmission line effectively compensates the amplitude and phase differences created within the balun by the difference in broadside coupler phase velocities, resulting in broadband operation. Additionally, this technique allows us to reduce the length of the coupler because of its broadband operation. The compensated balun previously measured realizes about 100% operating bandwidth and this performance is enough to design a broadband balanced frequency doubler MMIC.

Fig. 1 shows the equivalent circuit of the fabricated balanced frequency doubler MMIC. The size of each transistor used is 2 x 50 μm(gate width). Output 2nd harmonic signals from the drain are directly combined at the output junction. The length of the connecting lines, from the drain to the junction, were optimized to both maximize the output power and to realize broadband operation. The input matching circuit was constructed to obtain wider large-signal conjugate matching at the fundamental frequency. The output matching circuit was designed to realize broadband operation at 2nd harmonic frequency. The combination of the open stub and the short stub in the output matching circuit effectively realizes the 2nd harmonic signal gain and the fundamental signal suppression. Both matching circuits were optimized by using a harmonic balance analysis and a nonlinear FET model that considered the parasitic capacitance of the 3-D structure. The gate bias in near pinch-off region was set so as to obtain higher nonlinearity. In addition, the input and output matching circuits consist of inverted TFMS lines and TFMS lines, respectively and are stacked above and below a middle ground plane formed on the polyimide films (see Fig. 1) to achieve compactness. Fig. 2 shows a microphotograph of the fabricated balanced frequency doubler 3-D MMIC. The balun was formed using a meander configuration. The chip size of this MMIC is just 0.99 mm x 0.93 mm (intrinsic area is 0.66 mm x 0.62 mm).

IV. Measured Performance

Fig. 3 shows the measured performance of the fabricated balanced frequency doubler MMIC. The circles and triangles plot measured results while dotted line plots simulated results. These are in good agreement except at higher frequency. The doubler achieves 2.5 dBm ± 2.5 dBm output power and more than 15 dB fundamental signal suppression over 50 GHz to 68 GHz for 8 dBm input power. The maximum output power, 5 dBm, was measured with a conversion gain of -3 dB and a fundamental signal suppression of 23 dB at 61 GHz. The drain bias and the gate bias are 2.5 V and -0.6 V, respectively. The power consumption at 8 dBm input

TABLE I
State-of-the-art of V-band frequency doubler MMIC

Ref.	Type	Device	Band-width (%)	Chip size (mm^2)	Broadband factor (Bandwidth / chip size)	Output power (dBm)	f_0 suppression (dB)	Input power (dBm)	Drain bias (V)	Buffer amps., etc
This work	**Balance**	**0.15 μm GaAs pHEMT**	**30.5**	**0.92**	**0.33**	**2.5**	**> 15**	**8**	**2.5**	**-**
[1]	Single	0.1 μm GaAs pHEMT	5.0	2.61	0.019	2.5	-	-10	-	Input & output
[2]	Single	0.15 μm GaAs pHEMT	7.3	2.38	0.031	5	> 20	7	4	-
[3]	Single	0.5 μm InP pHEMT	-	4.59	-	1	-	-	-	-
[4]	Single	0.14 μm GaAs pHEMT	25.1	3	0.084	6	> 20	5	3	Output
[5]	Distributed	Diode	22.9	-	-	14.5	-	24	-	NLTL
[6]	Balance	0.15 μm GaAs pHEMT	24.4	1.79	0.14	0	> 20	14	2	-
[10]	Single	0.18 μm GaAs pHEMT	28.1	1.93	0.15	15.2	-	3	-	Output
[11]	Single	0.15 μm GaAs pHEMT	6.9	1.65	0.041	-1	> 15	3	3.3	-

power is 5 mW. Fig. 4 shows the measured output power as a function of the input power level at 50 GHz and 64 GHz. The saturated output power of the 2nd harmonic signal is more than 5 dBm at 50 GHz and 64 GHz.

Table I compares reported V-band frequency doubler MMICs to the fabricated balanced frequency doubler MMIC described herein. The fabricated MMIC exhibits substantially improved performance in terms of operating frequency bandwidth and reduced chip area. The broadband factor, defined as operating bandwidth (±2.5 dB deviation) per chip area, is twice those of reported V-band frequency doubler MMICs. These results indicate that the fabricated doubler MMIC is particularly suited to integration into single-chip transceiver MMIC because of its compactness and broad bandwidth. In addition, it can be used in various applications.

V. Application to 50-GHz Band Transmit MMIC

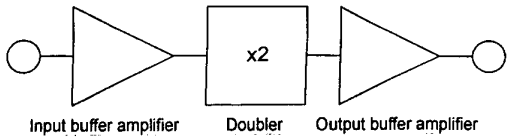
The developed balanced frequency doubler MMIC is easily applied to 50-GHz band transmit MMIC due to its small size and wide operation frequency range. Fig. 5 shows the fabricated transmit MMIC. This MMIC consists of a 25-GHz band input amplifier, the newly developed V-band frequency doubler, and a 50-GHz band output amplifier shown in Fig. 5 (a). A microphotograph of the fabricated MMIC is shown in Fig. 5 (b). The chip size of the MMIC is just 1.7 mm x 0.84 mm. The input amplifier consists of a 4 x 50 μm gate-width pHEMT and input and output matching circuits. The output amplifier consists of cascode-connected 4 x 50 μm gate-width pHEMT and matching circuits. The measured performance of this MMIC is shown in Fig. 6. The output power for a 25-GHz input signal is 10 dBm with an associated gain of 13 dB. An isolation of more than 40 dBc is obtained at this frequency. Supplied drain biases are 2.5 V for the input amplifier and the doubler and 5 V for the output amplifier. The power consumption is 300 mW.

V. Conclusion

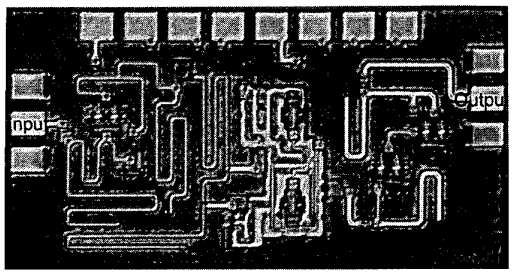
A compact and broadband V-band balanced frequency doubler MMIC was presented. The developed MMIC was manufactured by combining the UMS PH15 foundry process with the NEL 3-D MMIC interconnection process. The V-band doubler MMIC achieves both miniaturization and the widest frequency operation yet reported. Its broadband factor, 0.33, is twice those of reported doubler MMICs. A compact 50-GHz band transmit MMIC based on the V-band doubler was also demonstrated. The fabricated doubler MMIC will be very useful in realizing highly integrated MMICs.

Acknowledgement

The authors would like to thank Dr. Mizuno and Dr. Toyoda for their valuable suggestions and encouragement of this work. The authors also wish to acknowledge the great assistance and support of Mr. Taltasse and foundry department of United Monolithic Semiconductor S.A.S.,



(a)



(b)

Fig. 5. 50-GHz band transmit MMIC.
(a) Block diagram, (b) Microphotograph

Mr. Amano of Richardson Electronics K.K., and Mr. Ishikawa and Mr. Kondoh of NTT Electronics Corp.

REFERENCES

[1] A. Kanda, T. Hirota, H. Okazaki, and M. Nakamae, "An MMIC chip set for a V-band phase-locked local oscillator," *1995 IEEE GaAs IC Symp. Dig.*, pp. 259-262, Nov. 1995.

[2] M. Funabashi, T. Inoue, K. Ohata, K. Maruhashi, K. Hosoya, M. Kuzuhara, K. Kanakawa, and Y. Kobayashi, "A 60 GHz MMIC stabilized frequency source composed of a 30 GHz DRO and a doubler," *1995 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 71-74, May 1995.

[3] K. Sasaki, J. Utsu, K. Matsugatani, K. Hoshino, T. Taguchi, and Y. Ueno, "InP MMICs for V-band FMCW radar," *1997 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 937-940, June 1997.

[4] C. Fager, L. Landen, and H. Zirath, "High output power, broadband 28-56 GHz MMIC frequency doubler," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1589-1591, June 2000.

[5] E. Carman, M. Case, M. Kamegawa, R. Yu, K. Giboney, and M. Rodwell, "V-band and W-band broad-band, monolithic distributed frequency multipliers," *IEEE Microwave Guided Wave Lett.*, vol. 2, no. 6, pp. 253-254, June 1992.

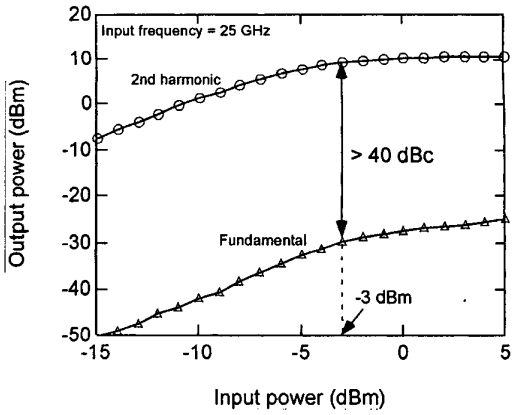


Fig. 6. Measured performance of transmit MMIC.

[6] B. Piernas, H. Hayashi, K. Nishikawa, K. Kamogawa, and T. Nakagawa, "A broadband and miniaturized V-band PHEMT frequency doubler," *IEEE Microwave Guided Wave Lett.*, vol. 10, no. 7, pp. 276-278, July 2000.

[7] K. Nishikawa, I. Toyoda, and T. Tokumitsu, "Compact and broad-band three-dimensional MMIC balun," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 1, pp. 96-98, Jan. 1999.

[8] K. Nishikawa, K. Kamogawa, K. Inoue, K. Onodera, T. Tokumitsu, M. Tanaka, I. Toyoda, and M. Hirano, "Miniaturized millimeter-wave masterslice 3-D MMIC amplifier and mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 9, pp. 1856-1862, Sept. 1999.

[9] M. Hirano, K. Nishikawa, I. Toyoda, S. Aoyama, S. Sugitani, and K. Yamasaki, "Three-dimensional passive circuit technology for ultra-compact MMICs," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 12, pp. 2845-2850, Dec. 1995.

[10] J. Mizoe, T. Matsumura, K. Unosawa, Y. Akiba, K. Nagai, H. Sato, T. Saryo, and T. Inoue, "A V-band GaAs MMIC chip set on a highly reliable Wsi/Au refractory gate process," 1997 *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 247-250, June. 1997.

[11] http://www.ums-gaas.com